TMC2243

CMOS FIR Filter

10 x 10 Bit, 20 MHz

Features

- 20 MHz data input and computation rate
- 10 x 10 bit multiplication with 23-bit extended precision sum of products (overflow, plus 16 output and 6 guard bits)
- Up to 3 zero and 3 non-zero stages per device
- Two's complement arithmetic
- 16-bit Sum-In and Sum-Out ports for cascading
- Internal 1/2 LSB rounding
- All inputs and outputs are registered
- One coefficient update per clock cycle
- Low power consumption CMOS process
- Single +5V supply
- Available in 68-pin ceramic pin grid array and 69-pin plastic PGA packages

Applications

- FIR filters
- Adaptive filters
- Multi-bit correlation
- One and two dimension video filtering
- Radar signal processors
- One and two dimension convolution
- Arithmetic element for systolic array processors

Description

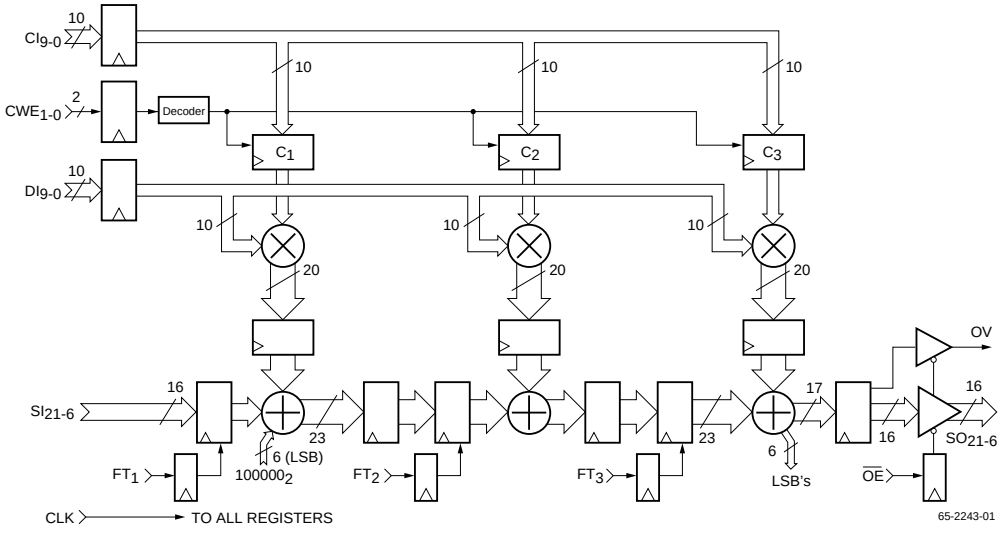
The TMC2243 is a video speed three stage 10 x 10 bit FIR (Finite Impulse Response) filter integrated circuit composed of three registered multiplier-adders concatenated into a one-dimensional systolic array. Utilizing two's complement representation, the TMC2243 accepts one 10-bit data point, updates one 10-bit coefficient, and produces one 16-bit rounded, filtered output point every 50 nanoseconds.

The TMC2243 has features which facilitate longer FIR filters: a 16-bit SUM-In port and user programmable pipeline registers. Enabling these registers allows the insertion of a zero-coefficient stage before each regular filter stage for up to six stages per TMC2243. Larger FIR filters can be built by cascading Sum-In and Sum-Out.

Coefficients are stored in 3 registers and are addressed via the 2-bit Write Enable control, allowing one coefficient to be changed per clock cycle. All Data, Sum-In, Sum-Out and instruction inputs are registered on the rising edge of clock.

The 16 bits below the MSB of the 23-bit internal summation path are available at the SUM-In and Sum-Out ports. Six bits of cumulative word growth are provided internally. Data Overflow is indicated by an output flag.

Block Diagram



Rev. 1.1.1

Functional Description

General Information

The TMC2243 consists of three identical arithmetic cells, each of which contains a 10 x 10 two's complement multiplier and a 23-bit adder. Each cell receives the current data (DI) from the Data input register, multiplies it by a locally stored Coefficient (CI_i), and adds it to the Sum $SI_{(i-1)}$ received from the previous cell. The result,

$$SI_i = DI \times CI_i + SI_{(i-1)},$$

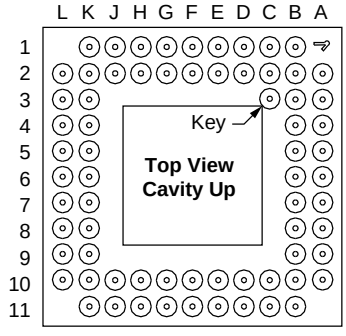
then goes to the next cell via two serial pipeline registers. When only one pipeline register is enabled, stages (i-l) and i are sequential. When both registers are enabled, there is a stage with a zero coefficient between them.

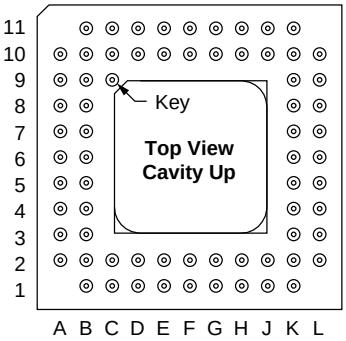
The input arithmetic cell receives $SI_{(i-1)}$ via the 16-bit Sum-In port (registered when FT_1 = LOW), filling the six lower bits with 100 000 (1/2 LSB) for internal rounding. The output cell outputs 16 of the MSBs (V_{21} through V_6) of SO_i through a register to the Sum-Out port. The Overflow flag is set when the final output exceeds 16 bits and resets with the output of the next nonoverflowing result. Sum-Out and the Overflow Flag can be forced to high-impedance with the Output Enable control. See Figure 1.

The two-bit Write Enable control specifies the loading of the three coefficient registers (one per arithmetic cell) with data appearing at the Coefficient Input port.

Pin Assignments

68 Pin Grid Array – G8 Package
69 Pin Plastic Pin Grid Array – H8 Package





Pin	Name	Pin	Name	Pin	Name	Pin	Name
A2	SO_6	B9	SO_{20}	F10	SI_{11}	K4	CI_2
A3	SO_7	B10	OV	F11	SI_{10}	K5	CI_4
A4	SO_9	B11	GND	G1	DI_6	K6	V_{DD}
A5	SO_{11}	C1	FT_0	G2	DI_7	K7	CI_7
A6	SO_{13}	C2	OE	G10	SI_{13}	K8	CI_9
A7	SO_{15}	C10	V_{DD}	G11	SI_{12}	K9	SI_{20}
A8	SO_{17}	C11	V_{DD}	H1	DI_4	K10	GND
A9	SO_{19}	D1	FT_2	H2	DI_5	K11	SI_{18}
A10	SO_{21}	D2	FT_1	H10	SI_{15}	L2	DI_0
B1	V_{DD}	D10	SI_7	H11	SI_{14}	L3	CI_1
B2	GND	D11	SI_6	J1	DI_2	L4	CI_3
B3	SO_8	E1	CWE_1	J2	DI_3	L5	CI_5
B4	SO_{10}	E2	CWE_0	J10	SI_{17}	L6	CI_6
B5	SO_{12}	E10	SI_9	J11	SI_{16}	L7	CI_8
B6	SO_{14}	E11	SI_8	K1	GND	L8	SI_{21}
B7	SO_{16}	F1	DI_8	K2	DI_1	L9	SI_{19}
B8	SO_{18}	F2	DI_9	K3	CI_0	L10	CLK

Note: Pin C3 is a mechanical orientation pin on the H8 package at manufacturer's option.

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Pin Descriptions

Pin Name	Pin Number	Description
Power		
V_{DD}	B1, K6, C10, C11	**Supply Voltage.** The TMC2243 operates from a single +5V supply.
GND	B2, K1, K10, B11	**Ground.**
Inputs		
DI_{9-0}	F2, F1, G2, G1, H2, H1, J2, J1, K2, L2	**Data Input.** DI_9 through DI_0 is the 10-bit registered Data Input; DI_9 is the MSB (sign bit) and DI_0 is the LSB. Data is in two's complement representation, and is clocked into the data register on each rising edge of clock. See Figure 1.
SI_{21-6}	L8, K9, L9, K11, J10, J11, H10, H11, G10, G11, F10, F11, E10, E11, D10, D11	**Sum Input.** SI_{21} through SI_6 is the 16-bit Sum-In port. SI_{21} is the MSB (sign bit). Sum-In is truncated to bit SI_6 (plus the 1/2 LSB rounding bit in SI_5) and is in two's complement representation. See Figure 1. The Sum-In port is registered, on the rising edge of clock, only when FT_1 =LOW. Unique input setup requirements must be observed when operating in the feedthrough mode (FT_1 = HIGH) See text.
CI_{9-0}	K8, L7, K7, L6, L5, K5, L4, K4, L3, K3	**Coefficient Input.** CI_9 through CI_0 is the 10-bit registered Coefficient Input; CI_9 is the MSB (sign bit) and CI_0 is the LSB. Each coefficient and its write enable address (CWE_{1-3}) are registered on the same clock. The coefficient is then latched into the indicated register (C_{1-3}) at the rising edge of the next clock. The contents of this bus are ignored if a coefficient register is not selected (CWE = 00). The format of CI_{9-0} is identical to that of DI_{9-0}.
Outputs		
SO_{21-6}	A10, B9, A9, B8, A8, B7, A7, B6, A6, B5, A5, B4, A4, B3, A3, A2	**Sum Output.** SO_{21} through SO_6 is the three-state 16-bit registered Sum-Out port; SO_{21} is the MSB (sign bit). For maximum precision, the internal products and accumulations are 23 bits but Sum-Out is internally truncated to 16 bits, and excludes the overflow bit and the 6 LSBs. The format is identical to that of SI_{21-6}. See Figure 1.
Clock		
CLK	L10	**Master Clock.** The TMC2243 has a single clock input. The rising edge of CLK strobes all enabled registers. All timing specifications are referenced to the rising edge of clock.
Controls		
CWE_{1-0}	E1, E2	**Coefficient Write Enable.** The two bits of the registered Coefficient Write Enable control indicate which of the coefficient registers is to receive a new coefficient at the beginning of the next clock cycle. **CWE_{1-0} Coefficient Register Selected** 0 0 Holds all coefficients unchanged. 0 1 C_1 1 0 C_2 1 1 C_3
FT_{3-1}	D1, D2, C1	**Feedthrough.** These registered Feed Through controls select clocked (FT_i = LOW) or feedthrough (FT_i = HIGH) operation for each of the pipeline registers. Setting FT_i = LOW inserts a zero coefficient stage, or additional register, before the ith non-zero stage.
$\overline{OE}$	C2	**Output Enable.** Output Enable is a registered three-state enable control which forces the Sum-Out port and Overflow to the high-impedance state when HIGH. These outputs are enabled when $\overline{OE}$ is LOW.
Flags		
OV	B10	**Overflow.** The Overflow Flag is a registered three-state output which goes HIGH whenever the summation result exceeds 16 bits and is reset to LOW on the next nonoverflowing result.

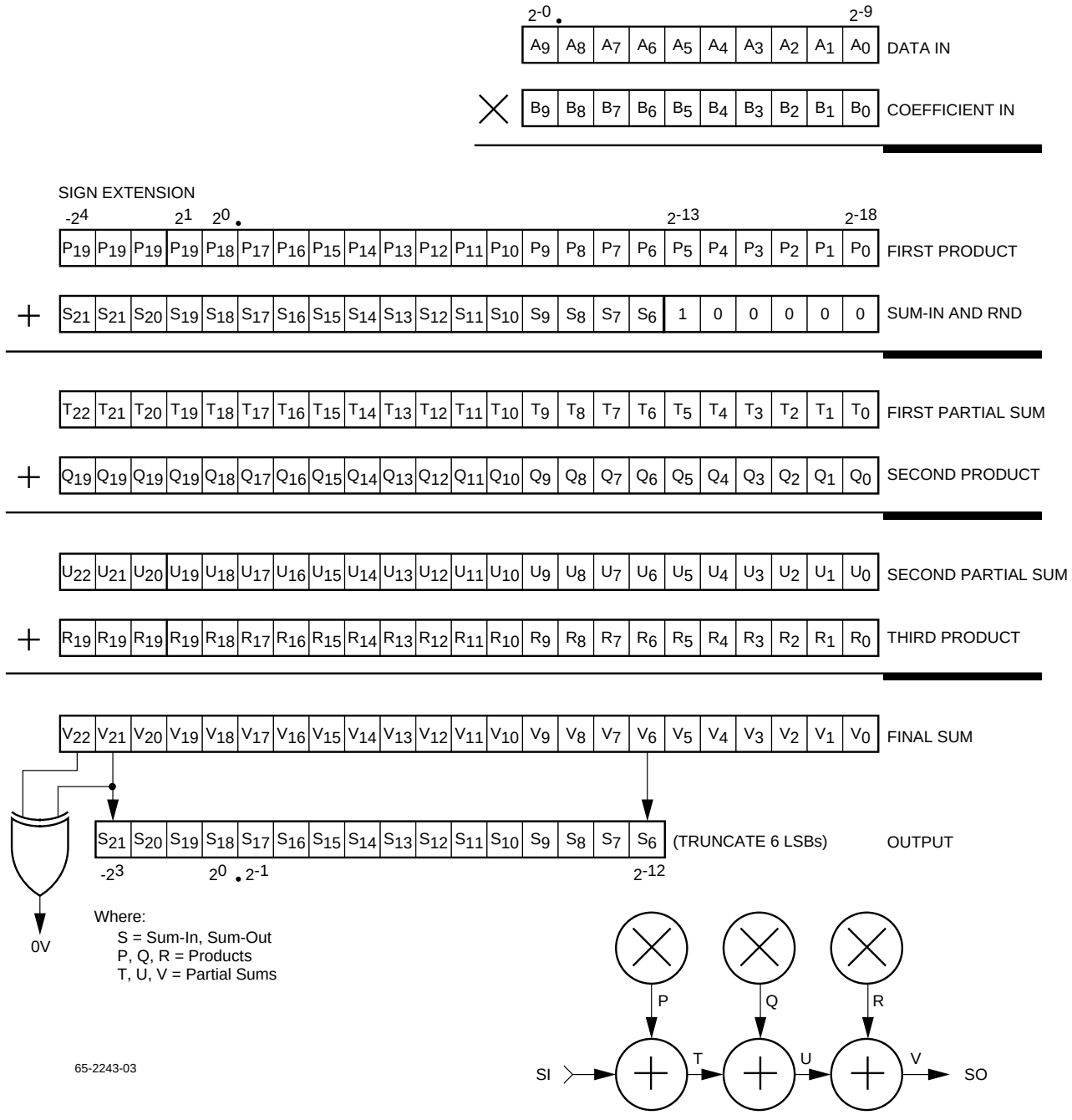
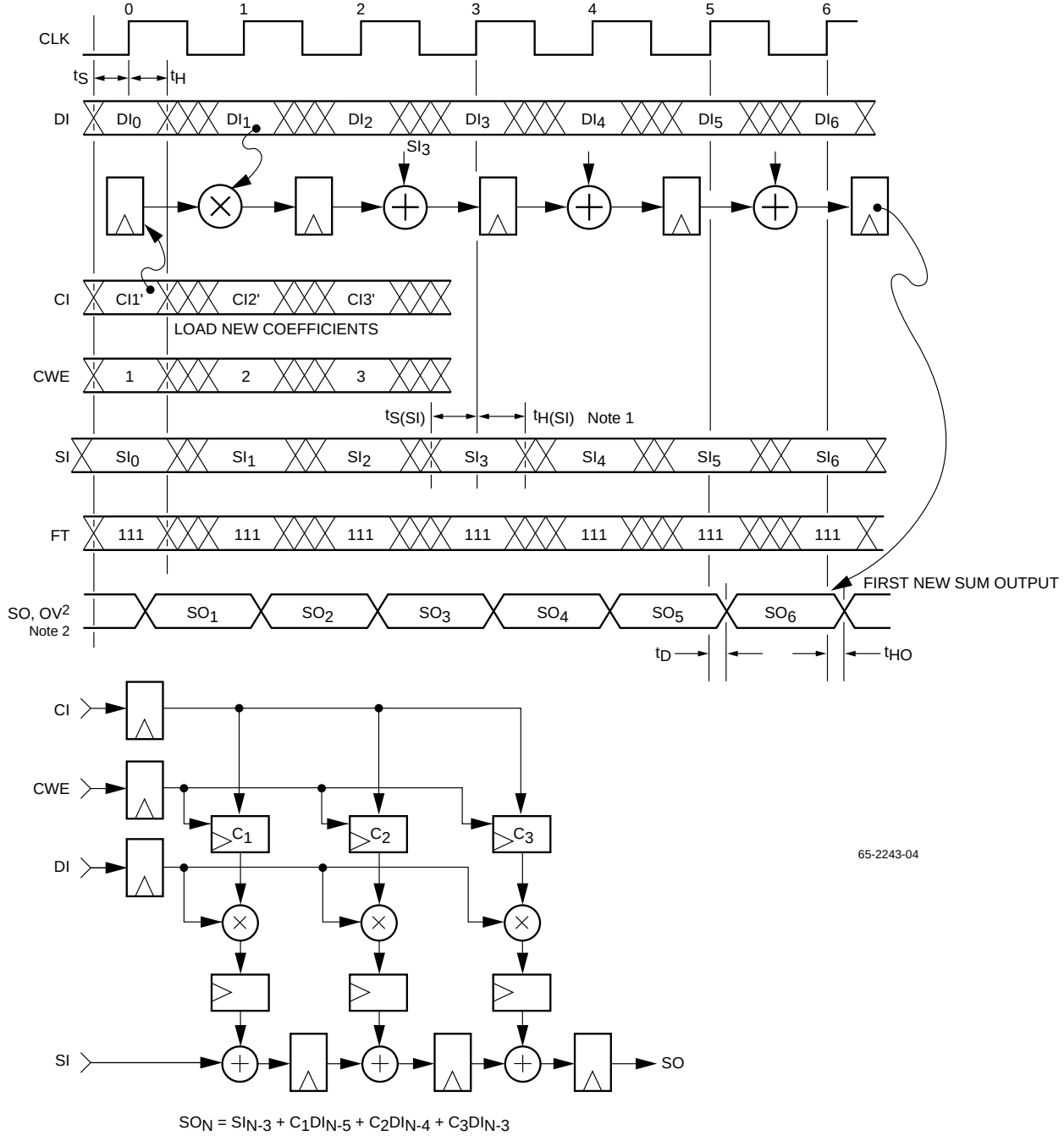


Figure 1. Data Formats and Internal Busing

Because the Sum-In and Sum-Out are truncated by 6 bits relative to the external accumulation pipeline, the TMC2243 rounds internally by adding 2^{-13} to each emerging sum of products, effecting half-LSB rounding relative to the output format. The chip internally utilizes all lower-order bits, to 2^{-18}.

Basic Operation



$$SO_N = SI_{N-3} + C_1DI_{N-5} + C_2DI_{N-4} + C_3DI_{N-3}$$

Notes:

1. Setup and Hold requirements for the Sum Input are similar to the other registered inputs when FT_1 = LOW. See text.
2. Sum Out and Overflow timing are shown with $\overline{OE}$ = LOW.

Figure 2. Timing Diagram Demonstrating Basic Operation with FT_{1-3} = HIGH (no zero stages)

The basic equation describing the function of the TMC2243 operating in a fixed state is:

$$SO(N) = SI_{(N-6+FT1+FT2+FT3)} + C_1 \times DI_{(N-7+FT2+FT3)} + C_2 \times DI_{(N-5+FT3)} + C_3 \times DI_{(N-3)}$$

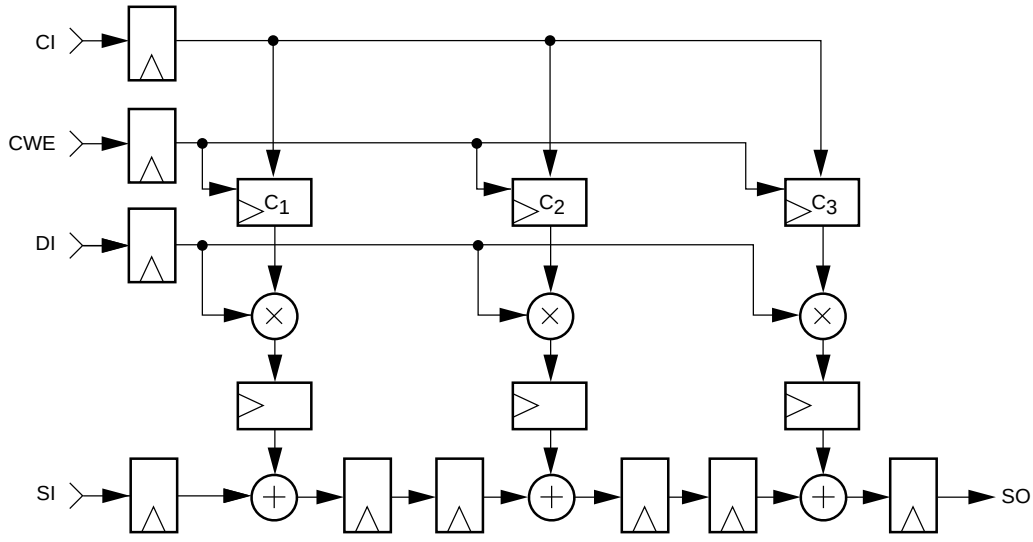
Careful observation of the clock delays shown is basic to construction of a filter algorithm. The operating sequence for the common application with FT_{1-3} = HIGH (no zero stages) is shown in Figure 2. The simplified block diagram demonstrates the clock stages in this configuration. When FT_1 = HIGH, the input feedthrough register is bypassed, and care must be taken to observe the setup requirements on the input of the first adder. Due to the absence of the input register buffer, note that the adder operates on data stable just prior to the arrival of the next clock, and not that setup at the rising edge of the current clock. When FT_1 = LOW the input register latches the input data, and the Sum Input follows setup and hold requirements similar to the other registered inputs of the TMC2243. When FT_1 = HIGH, $t_{S(SI)}$ is guaranteed to allow 20MHz pipelined operation, assuming that input setup is observed, including cascaded operation. See the AC Characteristics table and Figure 9 in the Applications Discussion section.

Figure 3 shows the effects of the feedthrough registers on filter operation, with two different configurations. The inputs are those presented at the corresponding rising edge of clock, excepting the delayed setup requirements of the Sum Input when FT_1 = HIGH. The outputs are those available up to and including the corresponding edge of clock. Applications utilizing the TMC2243's ability to modify coefficients dynamically are demonstrated in Figure 4, showing the operation of a typical adaptive filter. Note that the Sum Output will be zero in the first few clock cycles of all examples only if the Coefficient Registers are initialized to zero beforehand.

Cycle	SI(A) FT_1 = LOW	SI(B) FT_1 = HIGH	DI	CI	CWE	SO
1	0	0	0	K0	01	X
2	0	0	0	K1	10	X
3	0	0	0	K2	11	X
4	SI_0	0	DI_0	0	00	X
5	SI_1	SI_0	DI_1	0	00	0
6	SI_2	SI_1	$D1_2$	0	00	0
7	SI_3	SI_2	DI_3	0	00	DI_0K_2
8	SI_4	SI_3	DI_4	K_0'	01	DI_1K_2
9	SI_5	SI_4	DI_5	0	00	$DI_0K_1 + DI_2K_2$
10	SI_6	SI_5	DI_6	K_1'	10	$SI_0 + DI_1K_1 + DI_3K_2$
11	SI7	SI_6	DI_7	0	00	$SI_1 + DI_0K_0 + DI_2K_1 + DI_4K_2$
12	SI8	SI_7	DI_8	K_2'	11	$SI_2 + DI_1K_0 + DI_3K_1 + DI_5K_2$
13	SI9	SI_8	DI_9	0	00	$SI_3 + DI_2K_0 + DI_4K_1 + DI_6K_2$
14	0	SI_9	0	0	00	$SI_4 + DI_3K_0 + DI_5K_1 + DI_7K_2$
15	0	0	0	0	00	$SI_5 + DI_4K_0 + DI_6K_1 + DI_8K_2$
16	0	0	0	0	00	$SI_6 + DI_5K_0' + DI_7K_1' + DI_9K_2´$
17	0	0	0	0	00	$SI_7 + DI_6K_0' + DI_8K_1´$
18	0	0	0	0	00	$SI_8 + DI_7K_0' + DI_9K_1´$
19	0	0	0	0	00	$SI_9 + DI_8K_0´$
20	0	0	0	0	00	$DI_9K_0´$
21	0	0	0	0	00	0

Figure 3. Impulse Response Filter Operation Sequence with $FT_{2,3}$ = LOW

SI(A) is the sequence of Sum Input data with FT_{1-3} = LOW (three zero stages).



$SO_N = SI_{N-6} + C_1DI_{N-7} + C_2DI_{N-5} + C_3DI_{N-3}$

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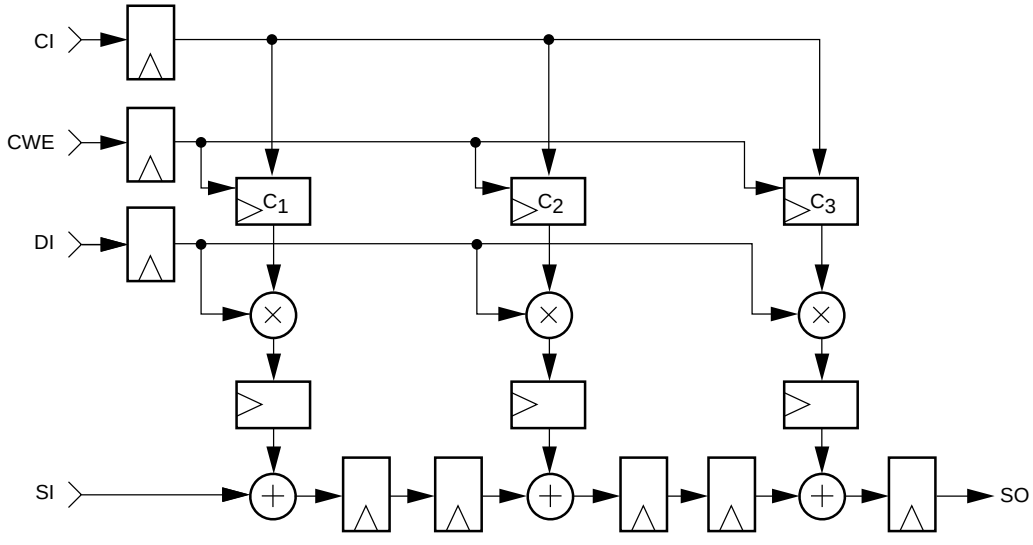
SI(B) is the sequence of Sum Input data with FT_1 = HIGH and $FT_{2,3}$ = LOW (two zero stages).



$SO_N = SI_{N-5} + C_1DI_{N-7} + C_2DI_{N-5} + C_3DI_{N-3}$

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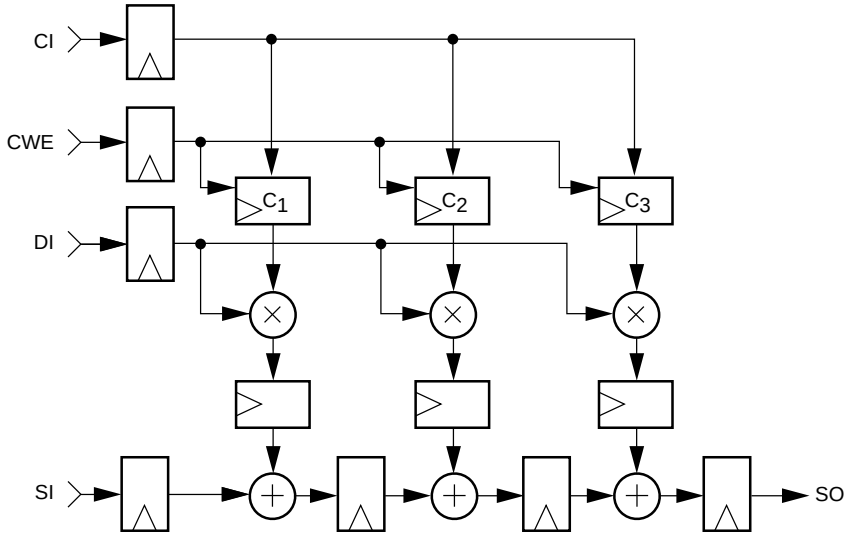
Cycle	SI	DI	CI	CWE	SO
0	SI_0	DI_0	A_1	01	X
1	SI_1	DI_1	A_2	10	X
2	SI_2	DI_2	A_3	11	X
3	SI_3	DI_3	B_1	01	X
4	SI_4	DI_4	B_2	10	X
5	SI_5	DI_5	B_3	11	X
6	SI_6	DI_6	C_1	01	$SI_2 + A_1DI_1 + A_2DI_2 + A_3DI_3$
7	SI_7	DI_7	C_2	10	$SI_3 + A_1DI_2 + A_2DI_3 + A_3DI_4$
8	SI_8	DI_8	C_3	11	$SI_4 + A_1DI_3 + A_2DI_4 + A_3DI_5$
9	SI_9	DI_9		00	$SI_5 + B_1DI_4 + B_2DI_5 + B_3DI_6$
10	SI_{10}	DI_{10}		00	$SI_6 + B_1DI_5 + B_2DI_6 + B_3DI_7$
11	SI_{11}	DI_{11}		00	$SI_7 + B_1DI_6 + B_2DI_7 + B_3DI_8$
12	SI_{12}	DI_{12}		00	$SI_8 + C_1DI_7 + C_2DI_8 + C_3DI_9$
13	SI_{13}	DI_{13}		00	$SI_9 + C_1DI_8 + C_2DI_9 + C_3DI_{10}$

Figure 4. Typical Adaptive Filter Operation Sequence

with FT_1 = LOW and $FT_{2,3}$ = HIGH (one zero stage)



$SO_N = SI_{N-4} + C_1DI_{N-5} + C_2DI_{N-4} + C_3DI_{N-3}$

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Equivalent Circuits and Transition Levels

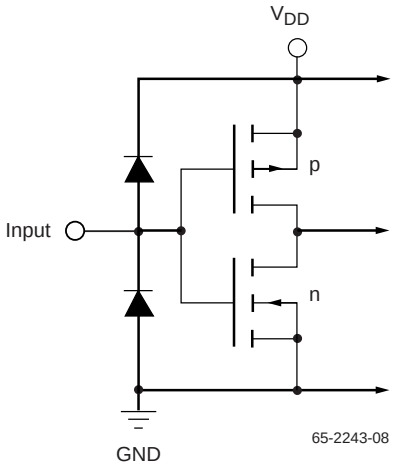


Figure 5. Equivalent Input Circuit

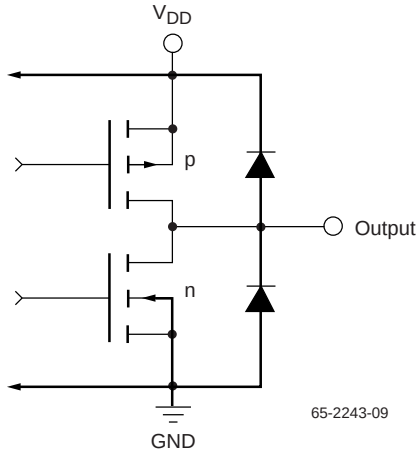


Figure 6. Equivalent Output Circuit

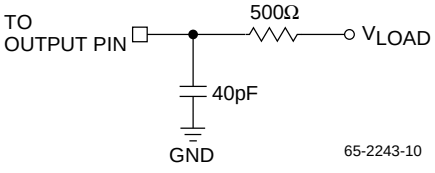
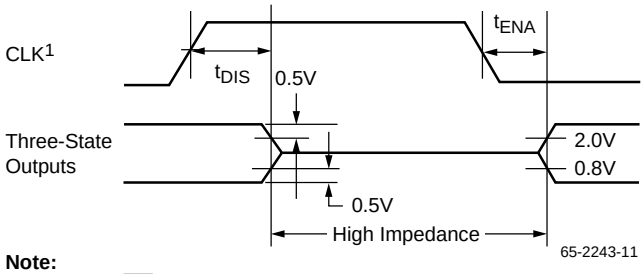


Figure 7. Test Load



Note:
1. Assumes $\overline{OE}$ has gone LOW, within the Input Setup requirements.

Figure 8. Transition Levels for Three-State Measurements

Absolute Maximum Ratings (beyond which the device may be damaged)[1]

Parameter	Min	Max	Unit
Supply Voltage	-0.5	7.0	V
Input Voltage	-0.5	VDD + 0.5	V
Output Applied Voltage[2]	0.5	VDD + 0.5	V
Output Forced Current[3,4]	-1.0	6.0	mA
Short circuit duration (single output in HIGH state to ground)		1	sec
Operating, Case Temperature	-60	130	°C
Operating, Junction Temperature		175	°C
Storage Temperature	-65	150	°C
Lead Soldering Temperature (10 seconds)		300	°C

Notes:
1. Absolute maximum ratings are limiting values applied individually while all parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range, and measured with respect to GND.
3. Forcing voltage must be limited to specified range.
4. Current is specified as conventional current flowing into the device.

Operating Conditions

Parameter		Test Conditions	Temperature Range						Units
			Standard			Extended			
			Min	Nom	Max	Min	Nom	Max	
V_{DD}	Supply Voltage		4.75	5.0	5.25	4.5	5.0	5.5	V
V_{IL}	Input Voltage, Logic LOW		2.0			2.0			V
V_{IH}	Input Voltage, Logic HIGH				0.8			0.8	V
I_{OL}	Output Current, Logic LOW				4.0			4.0	mA
I_{OH}	Output Current, Logic HIGH				-2.0			-2.0	mA
t_{CY}	Cycle Time	V_{DD} = Min	50			50			ns
t_{PWL}	Clock Pulse Width LOW	V_{DD} = Min	20			20			ns
t_{PWH}	Clock Pulse Width HIGH	V_{DD} = Min	20			20			ns
t_S	Input Setup Time		15			20			ns
$t_{S(SI)}$	Input Setup Time	SI_{21-6}, FT_1 = HIGH	25			28			ns
		FT_1 = LOW	18			20			ns
t_H	Input Hold Time		2			3			ns
$t_{H(SI)}$	Input Hold Time, SI_{21-6}		5			5			ns
T_A	Ambient Temperature, Still Air		0		70				°C
T_C	Case Temperature					-55		125	°C

DC Characteristics[1]

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
I_{DDQ}	Supply Current, Quiescent	V_{DD} = Max, V_{IN} = OV, $\overline{OE}$ = HIGH		15		15	mA
I_{DDU}	Supply Current, Unloaded	V_{DD} = Max, $\overline{OE}$ = HIGH					
		f = 20MHz		90		90	mA
		f = 10MHz		48		48	mA
I_{IL}	Input Current, Logic LOW	V_{DD} = Max, V_{IN} = OV	-75	75	-75	75	µA
I_{IH}	Input Current, Logic HIGH	V_{DD} = Max, V_{IN} = V_{DD}	-75	75	-75	75	µA
V_{OL}	Output Voltage, Logic LOW	V_{DD} = Min, I_{OL} = Max		0.4		0.4	V
V_{OH}	Output Voltage, Logic HIGH	V_{DD} = Min. I_{OH} = Max	2.4		2.4		V
I_{OZL}	Hi-Z Output Leakage Current, Output LOW	V_{DD} = Max, V_{IN} = OV	-40	40	-40	40	µA
I_{OZH}	Hi-Z Output Leakage Current, Output HIGH	V_{DD} = Max, V_{IN} = V_{DD}	-40	40	-40	40	µA
I_{OS}	Short-Circuit Output Current	V_{DD} = Max, Output HIGH, one pin to ground, one second duration max		-150		-150	mA
C_I	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF
C_0	Input Capacitance	T_A = 25°C, f = 1MHz		10		10	pF

Note:

1. Actual test conditions may vary from those shown, but guarantee operation as specified.

AC Characteristics

Parameter		Test Conditions	Temperature Range				Units
			Standard		Extended		
			Min	Max	Min	Max	
t_D	Output Delay	V_{DD} = Min, C_{LOAD} = 40pF		30		30	ns
t_{DC}	Output Delay, Cascaded	V_{DD} = Min, C_{LOAD} = 10pF		20		20	ns
t_{HO}	Output Hold Time	V_{DD} = Max, C_{LOAD} = 40pF	5		5		ns
t_{ENA}	Three-State Output, Enable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF		20		25	ns
t_{DIS}	Three-State Output, Disable Delay[1]	V_{DD} = Min, C_{LOAD} = 40pF		15		20	ns

Note:

1. All transitions are measured at a 1.5V level except for t_{DIS} and t_{ENA}.

Application Discussion

Loading and Updating of Coefficients

Because of the TMC2243's internal architecture, its impulse response is C_3, C_2, C_1, where C_3 is the rightmost coefficient and C_1 is the leftmost. However, for glitchless performance, coefficients must be updated from left to right: C_1 then C_2 then C_3.

For example, consider an adaptive filter whose first set of coefficients is A_i, second set is B_i and third set is C_i (Figure 4). First, the TMC2243 is initialized with A_i. If these are loaded in numerical (left to right) sequence, two of the first three data points can be loaded with them, as shown in Figure 4. Immediately after the third coefficient is loaded, the first coefficient of the next set can be loaded, if desired, along with the third data point.

Table 1. Impulse Response

FT_{3-1}	Response					
000	C_3	0	C_2	0	C_1	0
001	C_3	0	C_2	0	C_1	
010	C_3	0	C_2	C_1	0	
011	C_3	0	C_2	C_1		
100	C_3	C_2	0	C_1	0	
101	C_3	C_2	0	C_1		
110	C_3	C_2	C_1	0		
111	C_3	C_2	C_1			

Notes:

1. C_3 is she rightmost coefficient, C_1 is the leftmost
2. FT_1 is relevant only it SUMIN is used. When multiple chips are cascaded, FT_1 LOW places a zero stage between their concatenated impulse responses.

Building Longer Filters

To build a filter of more than three non-zero stages, merely concatenate a series of TMC2243s. The coefficient inputs may be connected to the data bus, a separate common coefficient bus, or separate buses, depending on system architecture, memory and bus resources, and coefficient updating requirements. The data inputs are connected to a common bus. If the first feedthrough register is used (and a zero stage is not desired there), an external register should be inserted in the data input path for proper timing (Figure 9).

The 16-bit Sum-Out port of each TMC2243 is connected to the Sum-In port of the next TMC2243 in the chain; the filter output is the Sum-Out port of the last TMC2243. Since the 6 LSBs of each TMC2243's accumulation pipeline are not output, each TMC2243 incorporates a rounding increment of 1 into the sixth bit, to minimize bias.

When TMC2243s are cascaded in this fashion, the minimum permissible clock period is the sum of the output delay and the Sum-In port's input setup time. When the Input Registers are enabled (that is, FT_1 = LOW), full 20MHz performance can be obtained.

All data and coefficient inputs and outputs are two's complement representation, whose relative scaling is presented in the Data Formats table, Figure 1. Although the data values are shown in fractional format, the user can arbitrarily rescale them, as long as consistency is maintained.

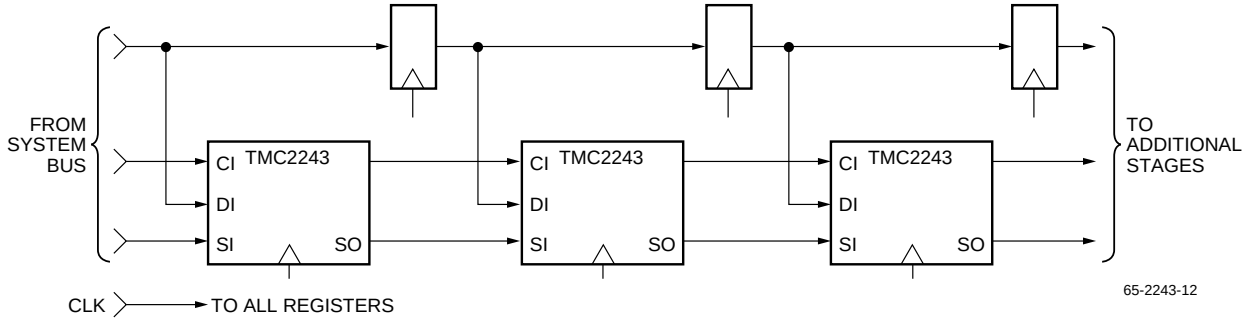


Figure 9. Basic Diagram for Stacking the TMC2243 for High–Speed Operation (no zero tap desired between each TMC2243, all FT_1 = LOW)

Notes:

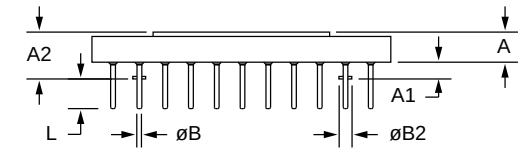
Mechanical Dimensions

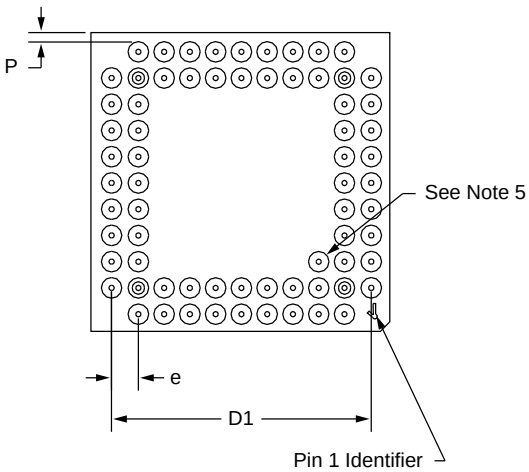
68 Lead PGA Package

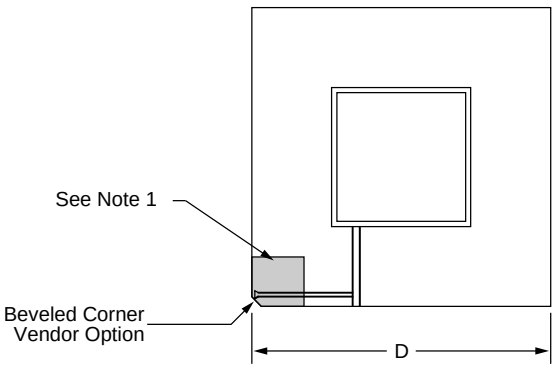
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.125	2.03	3.18	
A1	.040	.060	1.02	1.52	
A2	.115	.190	2.92	4.83	
øB	.017	.020	0.43	0.51	
øB2	.050 NOM.		1.27 NOM.		
D	1.140	1.180	28.96	29.97	
D1	1.000 BSC		25.40 BSC		
e	.100 BSC		2.54 BSC		
L	.120	.140	3.05	3.56	
M	11		11		2
N	68		68		3
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Dimension "M" defines matrix size.
3. Dimension "N" defines the maximum possible number of pins.
4. Controlling dimension: inch.
5. Optional index pin.







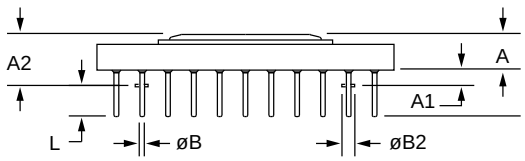
Mechanical Dimensions (continued)

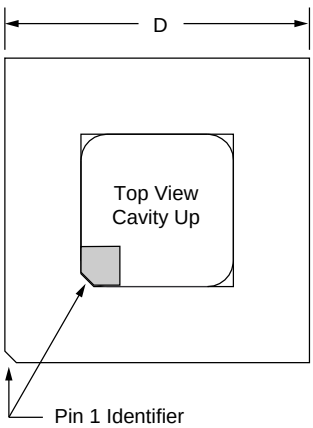
69 Lead PGA Package

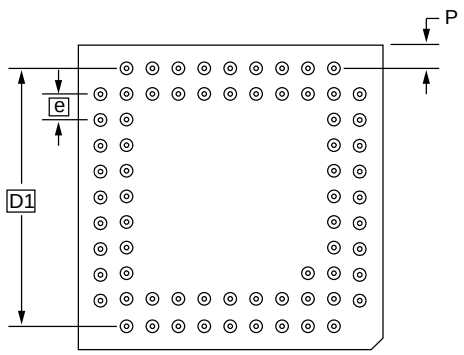
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.080	.160	2.03	4.06	
A1	.040	.060	1.01	1.53	
A2	.125	.215	3.17	5.46	
øB	.016	.020	0.40	0.51	2
øB2	.050 NOM.		1.27 NOM.		2
D	1.140	1.180	28.96	29.97	SQ
D1	1.000 BSC		25.40 BSC		
e	.100 BSC		2.54 BSC		
L	.110	.145	2.79	3.68	
M	11		11		3
N	68		68		4
P	.003	—	.076	—	

Notes:

1. Pin #1 identifier shall be within shaded area shown.
2. Pin diameter excludes solder dip finish.
3. Dimension "M" defines matrix size.
4. Dimension "N" defines the maximum possible number of pins.
5. Orientation pin is at supplier's option.
6. Controlling dimension: inch.







Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TMC2243G8C	STD-T_A = 0°C to 70°C	Commercial	68 Pin Grid Array	2243G8C
TMC2243G8V	EXT-T_C = 55°C to 125°C	MIL-STD-883	68 Pin Grid Array	2243G8V
TMC2243H8C	STD-T_A = 0°C to 70°C	Commercial	69 Pin Plastic Pin Grid Array	2243H8C

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